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EXAMINER	
MAI, ANH D	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 05/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/625,178	NAKAMURA, HIROKI	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *21-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 27-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Amendment

1. Amendment filed March 3, 2003 has been entered as Paper No. 18. Claims 1, 27 and 29 have been amended. Claims 1-33 are pending. Claims 21-26 have been withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 16-20, 29 and 31-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 16-20, Claim 16, lines 3-4, recites: a *bonding pad* formed on the semiconductor substrate in the circuit area; and a *fourth dummy pattern surrounding the bonding pad*".

Note that, claim 1, which claim 16 depends on, lines 5-7, recites: "a first dummy pattern ...., formed in the peripheral area, the dummy pattern encompassing the circuit area".

Since the fourth dummy pattern is surrounding the bonding pad, and the dummy pattern is formed in the peripheral area, then *the bonding pad is formed in the peripheral area*. However, this is contradicting the former limitation within claim 16, a *bonding pad* formed on the semiconductor substrate in the circuit area.

Claim 29 recites: "a peripheral area surrounding the circuit area; wiring patterns formed on the substrate in the circuit area, the wiring pattern including *a pad pattern*".

However, the pad pattern is formed between the dummy patterns, 600a and 600b. Therefore, the pad pattern is formed within the peripheral area.

Claim 29 is contradicting itself, thus indefinite.

Since claims 16-20, 29 and 31-33 are indefinite, further treatment on the merits could not be provided.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-3 and 27-33 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 27-41 of copending Application No. 10/128,244. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations: circuit area; wiring patterns and first dummy patterns is the same as: center area; first wiring pattern and second wiring pattern, respectively, of the copending application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-4, 11-15, 27, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaha et al. (JP-10-270445) in view of Hosoda et al. (JP-08-181208) all of record.

With respect to claim 1, Yamaha teaches a semiconductor device substantially as claimed including:

a semiconductor substrate (10) having a circuit area (RA) where an integrated circuit is formed and a peripheral area (RB);

wiring patterns (12) formed on the substrate (10) in the circuit area (RA);

a first dummy pattern (13) which is formed of the same material as the wiring pattern, formed in the peripheral area (RB);

a first insulating layer (14a) formed on the circuit area (RA) and the peripheral area (RB) of the semiconductor substrate (10);

a second insulating layer (14b) formed on the first insulating layer (14a) which is formed on the semiconductor substrate (10), wherein the second insulating layer (14b) is formed over the wiring pattern (12), and the second insulating layer (14b) is not formed over the first dummy pattern (13); and

a third insulating layer (14c) formed on the exposed first insulating layer (14a) and the second insulating layer (14b). (See Fig. 5).

Thus, Yamaha is shown to teach all the features of the claim with the exception of explicitly show that the dummy pattern (13) encompassing the circuit area (RA).

However, Hosoda teaches that the dummy patterns (14a) can be formed any where on a chip including surrounding the circuit pattern, hence peripheral area (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the dummy patterns (13) of Yamaha encompassing the circuit area (12) as taught by Hosoda to improve the planarity of the chip.

Regarding the wiring pattern (12) and the first dummy pattern (13) being formed of the same material, although not explicitly disclosed by Yamaha, however, it is well known in the art to pattern the first (12) and second (13) wiring patterns of Yamaha from a same deposited conductive material as shown by Hosoda to simplify the process.

Product by process limitation:

The expression "the width of the first (and third) dummy pattern is determined by the concentration of solid content of the SOG (claims 3, 9, 14 and 19); wherein the SOG layer has a certain concentration of solid contend; where a concentration of solid content of the SOG layer is around 5.2 wt% (claims 4, 10, 15 and 20); thermally planarized surface (claim 5)" are taken to be a product by process limitation and is given no patentable weight. A product by process claim

directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113 Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Note that, the solid content of the SOG only is only **existed before** being deposited or process step, on the semiconductor substrate, as a semiconductor device, the SOG layer after being deposited and cures, final product, is **no longer contained 5.2 wt %** as claimed.

With respect to claim 2, the second insulating layer (14b) of Yamaha is a SOG layer.

With respect to claim 3, insofar as the device is concerned, the first dummy pattern (13) of Yamaha has a width.

With respect to claim 4, insofar as the device is concerned, the width of the first dummy pattern (13) of Yamaha is designed for various size including less than 1μm.

With respect to claim 11, the device of Yamaha also includes: a third dummy pattern (13e) formed in the dummy area between the first dummy pattern (13d) and the wiring patterns (12).

Since the dummy pattern (13) of Yamaha can be a single wide pattern (13) or multiple narrower patterns (13a-e), therefore, the second insulating layer (14b) can be eliminated from the surface of the multiple dummy patterns as shown in fig. 5.

With respect to claim 12, the width of the third dummy pattern (13e) of Yamaha appears to be almost the same as that of the first dummy pattern (13d).

With respect to claim 13, there is a distance between the first (13d) and third (13e) dummy pattern of Yamaha. Since the dummy patterns (13a-e) are not used for connecting circuit elements, their sizes and spacing distribution can be selected freely.

Further, the claimed distance between the first and third dummy patterns of "exceeds 0.9μm" does not appear to be critical.

Note that the specification contains no disclosure of either the *critical nature of the claimed dimension of any unexpected results arising therefrom*. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claim 14, insofar as the device is concerned, the second insulating layer (14b) of Yamaha is a SOG layer.

With respect to claim 15, insofar as the device is concerned, the second insulating layer (14b) of Yamaha is a SOG layer and each of the first (13d) and third (13e) dummy patterns of

Yamaha. With respect to the size of the dummy patterns, the similar reason as that of claim 13 is also applied here.

With respect to claim 30, since the insulating layer (14b) of Yamaha is SOG, thus, the insulating layer (14b) of Yamaha inherently has a moisture absorbable characteristic.

With respect to claim 27, Yamaha teaches a semiconductor device substantially as claimed including:

a semiconductor substrate (10) having a circuit area where an integrated circuit is formed and a peripheral area surrounding the circuit area;

wiring patterns (12) formed on the substrate (10) in the circuit area (RA);

a dummy pattern (13) which is formed of the same material as the wiring pattern (12), formed in the dummy area (RB); and

an insulating layer (14b) formed above the semiconductor substrate (10), the insulating layer (14b) being formed over the wiring patterns (12), the insulating layer (14b) being formed outside the dummy pattern (13) but not being formed over the dummy pattern (13), and the insulating layer (14b) having a moisture absorbable characteristic. (See Fig. 5).

Thus, Yamaha is shown to teach all the features of the claim with the exception of explicitly show that the dummy pattern (13) encompassing the circuit area (RA).

However, Hosoda teaches that the dummy patterns (14a) can be formed any where on a chip including encompassing the wiring area (13) at the edge of the chip (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the dummy patterns (13) of Yamaha encompassing the wiring patterns (12s) as taught by Hosoda to improve the planarity of the semiconductor device.

Regarding the moisture absorbable characteristic, since the insulating layer (14b) of Yamaha is SOG, thus, the insulating layer (14b) of Yamaha inherently has a moisture absorbable characteristic.

With respect to claim 28, the insulating layer (14b) of Yamaha is a second insulating layer, the semiconductor device of Yamaha further comprises first (14a) and third (14c) insulating layers formed on the substrate (10), the second insulating layer (14b) being located between the first insulating layer (14a) and the third insulating layer (14c).

5. Claims 5, 6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaha '445 and Hosoda '208 as applied to claim 1 above, and further in view of Domae et al. (JP. Patent No. 09-283521) .

Yamaha and Hosoda are shown to teach all the features of the claim with the exception of explicitly disclosing the lower level of the semiconductor device.

However, Domae teaches a semiconductor device having multiple levels of metallization including:

a second dummy pattern (14) formed under the first dummy pattern (21); and

a fourth insulating layer (16) formed directly on the substrate (12) and on the second dummy layer (14), the fourth insulating layer (16) including a planarized surface,

whereby, the first dummy pattern (21) is formed on the fourth insulating layer (16) which is formed on the second dummy pattern (14), and the wiring pattern (15A) are formed on the fourth insulating layer (16). (See Fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the lower level of the metallization of Yamaha as taught by Domae to realize a high semiconductor integration density. (See Abstract).

With respect to claim 6, the shape and size of the second dummy pattern (14) is almost the same as that of the first dummy pattern (21).

With respect to claim 8, the second insulating layer (14b) of Yamaha is a SOG layer.

With respect to claim 9, insofar as the device is concerned, the first dummy pattern (21) and the second dummy pattern (14) of Domae of Yamaha has a width.

With respect to claim 10, insofar as the device is concerned, each of the first dummy pattern (21) and second dummy pattern (14) of Yamaha, in view of Domae, are designed for various size including less than 1μm.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaha '445, Hosoda '208 and Domae '521 as applied to claim 5 above, and further in view of Lee (U.S. Patent No. 5,789,313) of record.

Yamaha, Hosoda and Domae teaches a fourth insulating layer formed directly on the substrate.

Thus, Yamaha, Hosoda and Domae are shown to teach all the features of the claim with the exception of explicitly disclosing the fourth insulating layer being BPSG.

However, Lee teaches an insulating layer (18) formed directly on the substrate comprises BPSG.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the fourth insulating layer of Domae using BPSG as taught by Lee to passivate the circuit formed on the substrate.

Response to Arguments

7. Applicant's arguments filed March 3, 2003 have been fully considered but they are not persuasive.

Applicant argues: "the dummy pattern of Yamaha is formed in a region where a lower layer wiring (12) is not formed closely, **not in the peripheral area**".

However, the term "peripheral" means outer part, and in the art the term does not means active or inactive. The specification as shown in fig. 7A-B also embraces the active wiring being formed within the peripheral area. Applicant for his convenient, has completely ignored his disclosure.

With respect to the material of the dummy pattern being the same as the wiring pattern, as discussed in the rejection, it would have been obvious to one having ordinary skill in the art at the time of invention to pattern the wiring pattern (12) and the dummy pattern (13) of Yamaha from a same deposited conductive material as shown by Hosoda to simplify the process.

With respect to the insulating layer 14b, applicant argues: Yamaha does not disclose the second insulating layer being not formed over the first dummy pattern.

However, viewing Fig. 5, which is part of the disclosure, one having ordinary skill in the art should have concluded that, the second insulating layer 14b does not formed over dummy pattern 13.

With respect to the third insulating film 14c, Applicant appears to contend that the third insulating film 14c of Yamaha does not formed on the exposed first insulating layer 14a.

Again, Fig. 5, clearly shows that the third insulating layer 14c contacting the first insulating layer 14a, thus meet the limitation "formed on the exposed first insulating layer 14a".

Applicant then, concludes: therefore, it is impossible for Yamaha device to protect his device from moisture, which come into the circuit area through the SOG layer 14b.

This is clearly a conjecture since Applicant fails to provide any evidences to support his position. Secondly, the device of Yamaha meet the claimed limitations thus, it should function as claimed.

With respect to Hosoda, Applicant disagrees with the assertion that Hosoda teaches the dummy pattern 14a can be formed any where on a chip including surrounding the circuit pattern, hence peripheral area.

However, this is the fact and is shown in Fig. 3 of Hosoda. Secondly, as discussed above, the dummy pattern of the present invention also formed in both circuit area and peripheral area. (See Figs. 7A-B).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on

combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Note that, the teaching of the third insulating layer 14c formed on the exposed first insulating layer 14a is shown by Yamaha. Thus, the argument with respect to moisture prevention is amounted to compartmentalize the references.

With respect to the Product-by-Process limitation, as clearly discussed in the previous Office Action, the terms such as "determined by the concentration of solid content of the SOG layer" etc., are the Product-by-Process limitations because: as a device, the SOG layer is a 100 % solid. Insofar as the device is concerned, the structure includes: wiring patterns having a width and SOG layer between the wiring patterns.

Claim 1 is obvious over the combination of the references.

With respect to claim 3, Applicant asserts: any kind of objects on earth have a width.

This assertion is absolutely correct. Claim 3 recites: the first dummy pattern has a width" and the first dummy pattern 13 of Yamaha also has a width. And the "how it is determined" is the Product-by-Process. Since the device of Yamaha clearly comprises SOG layer formed therein, it meet the limitation of the claim. The claim does not contain a quantitative value for the width of the wiring.

With respect to claim 4, Applicant argues: Yamaha does not disclose that the first dummy pattern (13) is designed in a specific range including less than 1 μm.

However, Yamaha clearly teaches: in recent years, most of the wiring patterns are at most 2~3 μm wide and **submicron** (less than 1 μm) **wiring** are not uncommon. (See col. 5, lines 20-21).

With respect to claim 11, the subject matter is similar to claim 1, except for a dummy pattern, claim 11 recites multiple dummy patterns. Therefore, the formation of the dummy patterns in the peripheral have been established as previous discussion.

Applicant argues: as described above, the third dummy pattern (13e) is formed in the circuit area as well as the first dummy pattern because the area (RB) shows the circuit area.

However, the present specification discloses just that, the third dummy pattern 600a, is also formed in the circuit area. (See Fig. 7A).

Applicant also argues: in Fig. 6, the SOG layer 14b is formed on the third dummy pattern 13e, and the SOG layer 14b is also formed on the first dummy pattern 13 in Fig. 5 as explained above.

However, Yamaha clearly teaches that the thinning of the SOG at the dummy pattern 13 is the result of the SOG formed over a less dense region. (See col. 3, line 65-col. 4, line 8). Yamaha further teaches: "...Since the dummy wiring pattern 13a, 13b,... are not used for connecting circuit elements, their size and distribution can be selected freely. (See col. 7, lines 30-37).

Since the size of the dummy pattern is freely selected, thus, if only two of the dummy patterns is formed and space further apart, the formation of SOG on the two dummy patterns should be similar to that of a single dummy pattern as that of Fig. 5, which is not formed on the third dummy pattern.

With respect to claim 12, Applicant appears to contend that Yamaha does not describe that the width of the dummy patterns 13 to be the same.

However, the description of the article pictured can be relied on in combination with the drawings, for what they would reasonably teach one of ordinary skill in the art. *In re Wright*, 569, F.2d 1124, 193 USPQ 332 (CCPA 1977). In the description, as discussed previously, Yamaha teaches: "their size and distribution can be selected freely" and the drawing shows, multiple dummy pattern 13 similar in size. Thus, one of ordinary skill in the art should reasonably conclude that the dummy patterns 13 have similar width and it is easily achievable.

With respect to claims 14 and 15, a similar reasoning is also applied here.

With respect to claim 27, the scope of claim 27 and the argument with respect to claim 27 is somewhat similar to that of claim 1, therefore, the similar reasoning as that of claim 1 is also applied here.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

A.M
May 7, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800